Gradual Degradation under RF Overdrive of MESFETs and PHEMTs

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Abstract—This invited paper is based on a narrative summary and discussion of a number of referenced investigations concerning the gradual degradation under RF overdrive of MESFETs and PHEMTs. After introducing the background of the problem, its mechanism, models, analysis, as well as potential solutions are discussed.

I. Introduction

As the GaAs device technology matures, emphasis is increasingly placed on system application hence device reliability under real operating conditions. This is especially critical for RF power transistors and amplifiers which require a careful trade-off between performance and reliability. When these devices are driven into heavy gain compression in order to achieve the maximum power or efficiency, they often suffer from the so-called "power slump" problem which typically shows up as approximately 1 dB drop in output power over 1 000 h of RF operation.

TABLE I
Unique Failure Modes of Power MESFETs

Time	Failure Mode	Mechanism	Solution
Past	Instantaneous burn-out	Source-drain breakdown	n^+ contact with drain ledge
	Long-term catastrophic burn-out	Surface oxidation and decomposition	PECVD SiN passivation
	Gradual parametric degradation	?	RF burn-in of packaged device 250°C, 1 week dc wafer screen
Present		Hot-electron trap formation	R. T., 24 h
Future			Improved device Circuit model

Initially, power slump problem was thought to be an unique problem of GaAs devices. In fact, after overcoming problems such as metallurgical diffusion and electron-migration which are common to all semiconductor devices, failure modes unique to power MESFETs evolved according to a historical pattern [1]. Table I summarizes the evolution from instantaneous burn-out (infant mortality) to long-term burn-out (catastrophic failure), and, finally, gradual parametric degradation (graceful failure). This is actually an accomplishment because, giving sufficient stress, any device will degrade sooner or later if it does not burn-out. It is the device maker's responsibility to identify the window of safe operation and to continue to enlarge this window. However, since the mechanism for gradual degradation was n understood, a labor- and equipment-intensive RF burn-i procedure was required to qualify the devices made fro each wafer. Worse yet, device reliability for new applicatio was not predictable until extensive life tests were performe for each application. This is because, without knowing whic was the fundamental stress factor, it was impossible t quantify the stress level in each application.

II. Mechanism

Within the last few years, a hot-electron-induced gradu degradation mechanism in MESFETs was uncovered [2, 3 4]. Such a degradation mechanism has been known to tak place in a Si MOSFET in which hot electrons can be trappe in the gate oxide, causing its threshold voltage to shift. Fe suspected that in a GaAs MESFET, hot electrons can also b trapped in the SiN passivation between the gate and drain thereby decreasing the MESFET's transconductance witho affecting its threshold voltage [5]. As for the PHEMT because it is structurally similar to both a MOSFET and MESFET, the PHEMT predictably exhibits a mixed behavio [6]. However, for thermally stable and higher drain voltag PHEMTs, the hot-electron-induced degradation mechanism i increasingly critical.

TABLE II
Effects of Gate-Drain Surface Electron Traps

Effect	Manifestation
Increased surface depletion	Lower open-channel drain current, transconductance, and S_{21}
Increased series resistance and trap-emptying field	Higher knee voltage
Decreased gate-drain capacitance	Lower open-channel S_{22}
Increased surface leakage	Higher gate leakage current
Relaxed gate-drain field	Higher breakdown voltage

Under an RF overdrive, hot electrons are generated near the drain end of the channel where the electrical field is the highest. A few *lucky* electrons can accumulate sufficient energy to tunnel into the SiN passivation to form permanent traps there. The effects of such traps are summarized in Table II. Notice that, because the traps are located *above* the channel, there is usually no observable change in dc or small-signal parameters near the quiescent point. Further, because the traps are located *beside* the channel, Schottky-barrier height and ideality factor often remain constant. This selective change in device characteristics help distinguish hot-electron

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effects from thermal or environmental effects. In fact, the most distinct feature of hot-electron effects is a negative temperature dependence. This is because, when the channel is hotter, electrons undergo more scattering and, therefore, are less energetic.

III. Modeling and Analysis

With the development of a novel waveform probing technique [7, 8], RF-dc correlation was established making it possible to replace RF burn-in with an on-wafer, room-temperature, accelerated dc screening procedure [9]. The fundamental stress factor was found to be the instantaneous drain-gate voltage, or, the associated gate-drain reverse-breakdown current. Driving the device into heavy gain compression is a necessary but not sufficient condition for gradual degradation, because gain compression is usually the combined effect of bias, match, and drive. During the RF overdrive of a MESFET, the combination of bias, match, and drive must allow the RF load contour to reach the reverse-breakdown region to cause degradation. Whereas during testing the combination of bias, match, and drive must allow the RF load contour to reach the open-channel region to sense power degradation. Thus, under Class B or C operation a MESFET can undergo degradation without apparent loss of power. When the match is optimized for efficiency by maximizing the voltage swing, degradation is most likely to occur. Lower channel temperature achieved by pulsed drives may aggravate the degradation.

Without the actual waveforms, it is difficult to estimate the instantaneous drain-gate voltage due to the highly nonlinear characteristics of a FET under compression. However, since the drain and gate voltages are essentially out of phase, the peak drain-gate voltage can be approximated by the difference between the most positive and negative swings of the drain and gate voltages, respectively. For the last output stage of a power amplifier, the drain and gate voltage amplitudes can be approximately the same. Assuming the gate bias voltage is much smaller than the drain bias voltage in the absolute sense, it follows that the peak drain-gate voltage is approximately three times the drain bias since the drain voltage swing is approximately twice the drain bias. Therefore, the conventional approach of biasing the drain at one half of the breakdown voltage, while can lead to better instantaneous performance, may result in permanent degradation. A more conservative drain bias would be one third of the breakdown voltage.

Breakdown in a semiconductor is often a reversible process whereas trap formation in an insulator is often irreversible. The experiments of [5] involve gate-drain reverse-breakdown currents of the order of 0.1 to 100 mA/mm. By pushing the breakdown current up to this range, breakdown or other device characteristics do not change instantaneously and higher power performance can be gained. However, within 1 to 1 000 h, output power degradatio observable. The time it takes is inversely proportional to current stress density. Since the different current densi correspond to a very narrow range of drain-gate voltages, electron temperature distribution hence the probability trap formation is assumed to be constant. It follows that, the different current densities, eventually the same numbe reverse-breakdown electrons are required to cause the sa level of degradation. Therefore, similar to therm accelerated life tests, one can *electrically* accelerate h electron-induced degradation by increasing the current den then extrapolate the lifetime to the typical density in operations. The observation of [5] gave a convenient fig of merit against gradual degradation, namely, 1 A·h/cm 2×10^{22} q/cm reverse-breakdown electrons are required degrade these devices. This figure of merit is expected vary significantly for different device designs and fabricat processes.

Since trap formation, reverse breakdown, and elect luminescence are all induced by hot electrons, elect luminescence measurement was also used to monitor dev degradation during life tests, without interrupti electrical stress conditions [10]. In case the RF wavefor cannot be readily measured, electro-luminescence, especia that above the bandgap transition, serves as a conveni indicator of hot electrons. Table III summarizes how elect luminescence is used as a precursor for either burn-out gradual degradation. Using a microscope, elect luminescence can also indicate whether or not a multi-c device is being stressed uniformly. As stressing progress the electro-luminescence intensity tends to become m uniformly distributed, because where electron traps formed the breakdown voltage will also be increased there slowing down the degradation locally.

TABLE III
Electro-luminescence Modes of Power MESFETs

Bias Point	Location	Mechanism	Energy	Precursor
Open-channel	Gate-end of drain	Source-drain breakdown	1.4 eV	Catastrophi burn-out
Half-open	None	—	—	—
Pinched-off	Drain-end of gate	Gate-drain breakdown	1.4 eV 2.0 eV	Gradual degradatior

The distribution of trapped charges in the SiN w directly observed by a novel high-voltage electron-bea induced current technique [11]. This allowed us numerically simulate the trap effects using a two-dimensio device model [12]. By assuming a surface trap density of 1 cm^{-2} which is distributed between 0 to 0.1 μm from the g toward the drain, general agreement was achieved betwe the simulation results and empirical formulas [1 Comparing the number of reverse-breakdown electro required and the number of traps formed, it is concluded t

approximately only one out of 10^{15} electrons is *lucky* enough to form traps. The empirical formulas are listed in Table IV. Notice that, until greater confidence can be established for the simulation, the proportional constants in the formulas need to be empirically determined for each type of devices. For example, for the devices of [5, 6], the threshold energy for trap formation was found to be approximately 1.9 eV which is slightly higher than the impact-ionization threshold of [110] electrons in (001) GaAs.

TABLE IV
EMPIRICAL FORMULAS OF HOT-ELECTRON EFFECTS IN MESFETS

Parameter	Formula
Maximum channel field	$E_M \propto V_{DD}$
Gate-drain reverse-breakdown current	$I_{GD} \propto \exp(-\phi_I/q\lambda E_M)$
Electro-luminescence intensity	$I_{EL} \propto \exp(-\phi_I/q\lambda E_M)$
Trap-formation rate	$dn_T/dt \propto \exp(-\phi_T/q\lambda E_M)$
Transient-relaxation effects	$\Delta E_M \propto n_T$; $dn_T/dt \propto 1/n_T$
Channel-current reduction	$\Delta I_{MAX} \propto [t \exp(-\phi_T/q\lambda E_M)]^{0.5}$
Lifetime to 10% degradation	$\tau_{90} \propto \exp(\phi_T/q\lambda E_M)$

q: electron charge; λ: electron mean free path; ϕ_I: impact-ionization threshold; ϕ_T: trap-formation threshold; n_T: surface-trap density; t: cumulative stress time

The SiN passivation has been known to cause piezoelectric effects of opposite signs for FET channels of orthogonal orientations. However, MESFETs aligned along [110] and [1$\bar{1}$0] on the same wafer were found to degrade similarly under the same level of electrical stress. This implies that mechanical stress probably does not play a major role here.

It is conceivable that, similar to the case of MOSFETs, hot electrons are trapped at the GaAs-SiN interface instead of in SiN. However, observations to date support the latter, probably because the interface state density of GaAs is very high in any case. The observations include: (i) The type of passivation material matters, but not the deposition method. (ii) Hot-electron-induced traps have a time constant of the order of 10 μs while typical interface states $\sim$1 μs. (iii) The threshold energy for gradual degradation is significantly higher than the bandgap of GaAs. (iv) Once the MESFET degrades, it cannot recover by deep-UV irradiation or 200°C anneal which are known to affect the interface states. (v) Partial recovery was found after partial etching of SiN. (vi) Although the recovery was incomplete after complete etching of SiN, etching damage on both the source and drain sides of the channel was revealed by high-voltage electron-beam-induced current.

IV. POTENTIAL SOLUTIONS

Based on the understanding of the degradation mechanism, work is now concentrating on improving the device design to reduce its degradation tendency. Common approaches involve optimization of channel doping and geometry for the best combination of breakdown voltage and power capacity. This is typically done by trial and error and may take many iterations of wafer processing and device characterization. However, with two-dimensional device modeling and its validation by high-voltage electron-beam-induced current, it is now possible to optimize the shape of the electrical rather than physical channel without many iterations.

Improvement or replacement of SiN as a surface passivation is another obvious approach. However, there have been conflicting reports of the superiority of SiN to SiO_2 [2] or vice versa [3]. Obviously, perfect passivation of the GaAs surface is yet to be found.

Delivering high power with high current thus limiting the operating voltage is not always feasible, especially for system designs that are accustomed to high supply voltages such as those traditionally served by vacuum tubes or bipolar transistors.

If the breakdown voltage is improved by adding a low-doped drain region as is common in a MOSFET, it may help constrict the MESFET channel thereby making it more susceptible to hot electrons. As device dimensions continue to shrink, hot-electron effects will only become more prevalent. They have already been observed in digital MESFETs operating under a few volts [2].

Attempts to improve device reliability against hot-electron effects have been complicated by different responses of dc and RF breakdown voltages to electrical stresses [14]. Using the waveform probing technique again, work is underway to extract and validate large-signal transistor models which include breakdown characteristics that cannot be readily measured by dc techniques [15]. The ultimate goal is to incorporate such device models into circuit simulators, so that circuit designers can quantitatively trade performance for reliability [16]. It will also allow us to predict the stress level hence device reliability in new applications, without application-specific waveform or burn-in tests.

To illustrate the above discussed procedure, the breakdown characteristics of [5] has been fitted to an empirical formula similar to that of [17]:

$$I_{GD} = -\exp[0.69(V_{DG}-11)] \qquad (1)$$

Figure 1 shows the gate current and drain-gate voltage waveforms measured from a 0.4 mm-wide MESFET which was driven with an input power of 20 dBm at 2 GHz. Because of the large input capacitance of the MESFET, the gate current is dominated by the displacement current which is basically symmetric with respect to the horizontal axis. The top gate-current swing is followed by a peak caused by forward Schottky conduction. The bottom gate-current swing is followed by a broad shoulder caused by reverse gate-drain breakdown. In comparison, the drain-

gate voltage waveform is smoother hence can be measured more accurately. By applying (1) to the drain-gate voltage waveform, the gate-current shoulder is replicated as shown in Fig. 1. The time average of (1) is calculated to be −3.7 mA or −9.3 mA/mm. According to the figure of merit discussed earlier, this device should degrade in approximately 10 h. Experimentally it was observed to degrade after 30 h, within the predicted order of magnitude.

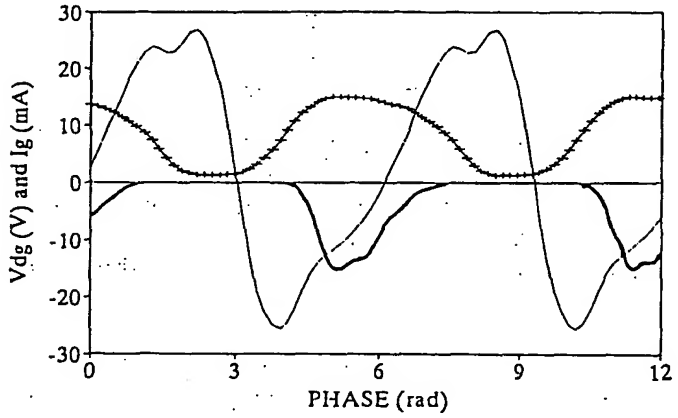

Fig. 1 Measured (—) gate current and (+) drain-gate voltage waveforms and (—) calculated gate-drain reverse breakdown current of a 0.4 mm-wide MESFET. V_{GS} = −3 V. V_{DS} = 7 V. P_{IN} = 20 dBm @ 2 GHz.

V. Conclusion

Hot-electron-induced trap formation has been found to be the cause of gradual degradation under RF overdrive of MESFETs and PHEMTs. The fundamental stress factor was found to be the instantaneous drain-gate voltage, or the associated gate-drain reverse-breakdown current. Therefore, the transistors can be screened at wafer level by subjecting them to different dc drain-gate voltages while observing the change in selected device characteristics. However, this is only a measure of transistor reliability or technology robustness. To predict the lifetime of a power amplifier against gradual degradation, the internal RF waveforms which the transistors are subjected to must be either directly measured or accurately simulated for the different overdrive conditions.

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